REMARKS

I. Status

In the Final Office Action mailed October 1, 2003, the Examiner noted that claims 1-6 were pending and rejected claims 1-6. The applicant respectfully traverses the rejection.

II. Oath Declaration

It is not required by the statutes or by the related rules to state a domestic priority claim in the declaration. To claim domestic priority under 35 U.S.C. 120, applicant must comply with 37 CFR 1.78 which requires, in part, that the priority claim information be in either the first line of the specification or in an application data sheet. 37 CFR 1.78 (2) (iii). The specification was amended in the Amendment of July 8, 2003 to include domestic priorities.

III. Foreign Priority

A certified copy of the priority document GB 9504046.5 has been ordered and will be submitted to the U.S. Patent Office when received.

IV. Double Patenting

The applicants submits a terminal disclaimer for the purpose of overcoming the double patenting rejection of U.S. Patent 6,122,315. However, Applicants do not admit to any characterization or limitation of the claims by the Examiner, particularly any that are inconsistent with the language of the claims considered in their entirety and including all of their constituent limitations.

V. Response to Examiner's "Response to Amendment"

As to points (5) and (6), the Examiner alleges that Horvath discloses a process-pipeline architecture to process different standards. The applicants respectfully disagree. The Examiner points out that Horvath discloses stages to process different standards[e.g. MPEG, JPEG] [col 1, lines 33-41; and col 10, lines 17-37].

The section referred to by the Examiner is in the Background of the Invention of Horvath et al., as follows

> "Image compression and decompression (CODEC) techniques, such as those referred to as the Joint Photographic Experts Group (JPEG) and the Motion Picture Experts Group (MPEG), make use of a discrete cosine transform (DCT) function. These techniques divide an image into many small areas, referred to as blocks..."
>
> column 1, lines 33-38

The above section of the Background merely refers to the existence of different standards and is recited for Background never relating this information to any embodiment of the invention.

Therefore, the above does not disclose as recited in claim 1 of the present invention "stages being reconfigurable to operate according to the different standards" (column 1, lines 3-4).

In fact, Horvath clearly discloses a machine which operates only on a single standard. For example, Horvath et al. states:

> "As was noted above, for the baseline JPEG method that is employed in the presently preferred embodiment, the Huffman coder is used to reduce the entropy of quantized DCT coefficients."

column 6, lines 24-28

Furthermore, Horvath et al. states that "[a] presently preferred DCT approach is one based on the Joint Photographic Experts Group (JPEG) baseline" (column 3, lines 54-56).

These sections of Horvath et al. clearly demonstrate that a single "standard" , in this case JPEG, is being processed in a preferred embodiment. This is clearly different then the present invention which can process a stream containing different standards or, alternately, multiple streams, with each stream containing a different standard. Horvath et al. does not disclose a device which has this functionality.

As to points (7) and (8), the Examiner alleges that Horvath discloses a "pipeline stage" including a "state machine". The applicant respectfully disagrees. The present invention recites to "pipeline stages being reconfigurable" (claim 1, lines 3-4). One example of an embodiment of a reconfigurable processing stage is described in the specification in section 6. RECONFIGURABLE PROCESSING STAGE on page 103, line 19 to page 109, line 33. The Examiner has cited column 2, lines 19-54 of Horvath et al. for disclosing processing circuitry which is used to process blocks of data. However, Horvath et al. does not show circuitry capable of "reconfiguration" and in particular "reconfiguration" in response to a different standard. As shown above, Horvath et al. only processes the data of a single standard.

As to points (9) and (10), the Examiner rejects applicants' argument that Ueda does not process image blocks. The applicants respectfully disagree.

As discussed below in the applicants response to the Examiner's rejection, Ueda is a machine directed to processing machine instructions, whereas Horvath et al. is an image processing system which processes image blocks. Thus, not only the inventions cannot be logically combined, but the Examiner offers no evidence of motivation in the prior art for combining these two unrelated devices.

Additionally, the reference Ueda is nonanalogous art. "In order to rely on

a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned". (MPEP 2141.01(a)). Ueda does not meet the first requirement of being in applicant's field of art because the present invention is directed to decoding of image data, voice data, and other data, whereas Ueda is directed to processing of machine instructions. Ueda does not meet the second requirement of being analogous art because a pipeline directed to processing machine instructions has no relevance to the decoding of image data, voice data, or other data.

As to points (11) and (12), the Examiner alleges that Horvath discloses a "token" because Horvath discloses "block processing". The applicants respectfully disagree.

A "token" of the present invention is defined as:

> "...A universal adaptation unit in the form of an interactive interfacing messenger package for control and/or data functions."
>
> specification, page 24b, lines 11-13

This entails a technology more powerful than a traditional token, for example, in the context of token rings, or a traditional packet of information. An embodiment of a token is described in section 10 TOKENS in the specification from page 120, line 30 to page 125, line 4. In contrast to the present invention, the sections of Horvath et al. disclosed by the examiner only shows "block processing" in a single standard. Horvath et al. does not disclose a "token" as defined in the specification as shown above. A token is a versatile structure having among its many capabilities, a multi-standard token, as described as follows:

> "[a] multi-standard token is a way of mapping MPEG, JPEG and H.261

data streams onto a single decoder using a mixture of standard dependent and standard independent hardware and control tokens"

specification, page 121, lines 17-20

As to points (13) and (14), the Examiner alleges that Ueda discloses an "inactive state". The applicants respectfully disagree. As discussed above, Ueda is nonanalogous prior art. Alternately, section 17, column 11-13 of Ueda does not appear to disclose a "predetermined activation pattern", but rather appears to disclose a pre-branching routine of a pipeline. The applicant requests that the Examiner point out how this section of Ueda discloses a "predetermined activation pattern" as recited in claim 1 of the present invention.

As to points (15) and (16), the Examiner alleges that Schwartz a pipeline stage as recited in claim 1. The applicants respectfully disagree. Schwartz is not in the applicant's field of art: the applicants device being for decoding a data stream; the device of Schwartz being a computer system for audio video digital recording and playback. Furthermore, Schwartz is not pertinent to the present invention because the data structures of Schwartz directed to processing analog and video information for playback have no relevance to decoding a data stream.

VI. Rejection of claims under 35 U.S.C. § 103(a)

Claims 1-2 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Horvath et al. in view of Ueda et al.

To support the allegation that Horvath et al. discloses at least one of the pipeline stages being reconfigurable to operate according to different standards, the Examiner cites to column 2, lines 45-55 and column 9, lines 13-38 of Horvath et al. Column 2, lines 45-55 of Horvath et al. teaches the storage of the data associated with an image block along with the control information for that image block. Similarly, column 9, lines 13-38 of Horvath et al. teaches a

"method for sequentially processing a plurality of data block" (column 9, lines 32-34). However, the above-stated sections of Horvath et al. does not disclose a "sequence of pipeline stages" (claim 1, line 3) nor does it disclose a pipeline stage which is "reconfigurable to operate according to...different standards" (claim 1, line 4). In fact, Horvath et al. teaches a sequential process (column 9, line 33) for operating on blocks of data in a buffer memory. Furthermore, the disclosure is silent as to the processing of different standards.

To support the allegation that Horvath et al. discloses the at least one of the pipeline stages including processing circuitry with an active state which is entered when the data received by the at least one of the pipeline stages has a predetermined activation pattern corresponding to on of the different standards, the Examiner cites to Figure 1, element 18, column 4, line 61 to column 5, line 30, and column 6, lines 1-16. Figure 1, element 18 shows a local state machine (LSM) which is used to coordinate the processing of image blocks and the decode process (column 5, lines 1-2). Column 4, line 61 to column 5, line 30 discloses how the LSM passes blocks of data to the CODEC 24. Column 6, lines 1-16 discloses the steps of a single standard, i.e the JPEG standard. Consequently, the above-stated sections of Horvath et al. show the interactions between the LSM and CODEC and do not disclose a pipeline stage, or a pipeline stage with an "active state" entered when the data has a "predetermined activation pattern" (claim 1, line 7). Furthermore, Horvath et al. is silent as to processing of "different standards" (claim 1, line 8) and the cited section column 1-16 does not disclose "different standards" but disclosing the steps of a single standard, namely the JPEG standard.

To support the allegation that at least one of the pipeline stages includes a state machine having a current state and a previous state, the Examiner cites to sections column 1, lines 59-61 and column 5, lines 15-30. Column 1, lines 59-61 discloses decoding of blocks of image data. Column 5, lines 15-30 discloses how the LSM reading data from the Input FIFO 28 and how the data is transferred to the CODEC. Thus, the above-mentioned sections of Horvath et al. merely disclose the coordinating steps between the LSM and CODEC in

processing image blocks, and do not disclose a "pipeline stage" including a "state machine".

The Examiner concedes that Horvath et al. does not disclose, inter alia, a sequence of pipeline stages. The Examiner provides the reference Ueda et al., particularly Figure 4, for its disclosure of a sequence of pipeline stages. However Ueda et al. discloses a pipeline architecture having fetch, decode and execute stages, used to process machine instructions. Ueda et al. is silent as to processing image processing blocks, and in fact would not work in processing image blocks since it is a different architecture designed to process machine instructions.

Furthermore, Ueda et al. processes machine instructions using an instruction fetch (IF) stage, a decoding stage (D), and address calculation stage (A) and an operation fetch stage (F). In contrast, Horvath et al. disclose a machine architecture for processing image blocks by the coordinated actions of an LSM and CODEC processors operating on image blocks stored in buffers. Thus, the machines would not work together, one being designed to process image blocks using primarily two processors and the other using several stages of a pipeline to process machine instructions.

Furthermore, the cited prior art does not disclose a "token" as recited in the claims of the present invention. A token of the present invention is defined in the specification as "interactive interfacing messenger package for control and /or data functions." This entails a technology more powerful than a traditional token, for example, in the context of token rings, or a traditional packet of information.

As to claim 2, Ueda discloses a bypass circuit allowing a memory fetch and write cycle to use the same data retrieved from memory without accessing the memory again. Ueda et al. does not disclose an "inactive state" (claim 2, line 2).

Therefore, the present invention recited in claims 1 and depending claims therefrom is not rendered obvious by the cited prior art.

VII. Rejection of claims under 35 U.S.C. § 103(a)

Claims 3-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Horvath et al., in view of Ueda et al. and further in view of Schwartz. The Examiner concedes that Horvath and Ueda do not disclose the sequence of pipeline stages including at least one spatial decoder stage or one temporal decoder stage. The Examiner cites to Schwartz for this disclosure. However, Schwartz shows a microcomputer system for converting an analog signal into a digital form and storing it in a highly condensed code. To achieve this goal, Schwartz operates on streams of data, in contrast to Horvath et al. which operates on image blocks. Furthermore, Schwartz does not require the data to conform to any standard. Thus, the machines of Horvath et al and Schwartz being directed to different goals and operating on different data structures are not combinable. Additionally, Ueda, designed to process machine instructions is unrelated to Schwartz which is processing streams of audio or video data.

Therefore, the present invention recited in claims 3-6 is not rendered obvious by the cited prior art.

VIII. Concluding Matters

In view of the foregoing remarks and amendments, it is respectfully submitted that each of the claims distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of allowance of all the pending claims is respectfully requested.

Should there be any remaining questions to correct format matters, it is urged that the Examiner contact the undersigned attorney with a telephone interview to expedite and complete prosecution.

If any further fees are required in connection with the filing of this response, please change same to our Deposit Account No. 04-1175.

Respectfully submitted,

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Date: 12/23/03

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